SEMI DESIGN

APPLICATIONS FOR SUMMER INTERNSHIP PROGRAM 2024

Hands-on Project Experience, Work on real projects that make an impact

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+91-9599745251

Visit Our Website
www.semidesign.in

SUMMER INTERNSHIP PROGRAM 2024

SEMI DESIGN

List of Projects

- DESIGN OF LOW POWER ADDER AND MULTIPLIER USING REVERSIBLE LOGIC GATES
- A NOVEL ULTRA-COMPACT FPGA-COMPATIBLE TRNG ARCHITECTURE EXPLOITING LATCHED RING OSCILLATORS
- DESIGN AND IMPLEMENTATION OF SUBWAY AUTOMATIC TICKETING SYSTEM BASED ON VERILOG HDL
- AN ULTRA-EFFICIENT APPROXIMATE MULTIPLIER WITH ERROR COMPENSATION FOR ERROR-RESILIENT APPLICATIONS
- HIGH-PERFORMANCE ACCURATE AND APPROXIMATE MULTIPLIERS FOR FPGA-BASED HARDWARE ACCELERATORS
- VLSI IMPLEMENTATION OF SPEED SINGLE PRECISION FLOATING POINT UNIT USING VERILOG
- AREA REDUCTION AES ALGORITHM IN HARDWARE TROJAN DETECTION
- TROT: A THREE-EDGED RING OSCILLATOR-BASED TRUE RANDOM NUMBER GENERATOR WITH TIME-TO-DIGITAL CONVERSION

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List of Projects

- VLSI IMPLEMENTATION OF VEDIC MULTIPLIER
- ANALYSIS OF KEY-BASED CRYPTOGRAPHIC ALGORITHMS AND ITS APPLICATIONS
- MULTI-CAR PARKING SYSTEM USING VERILOG
- APPROXIMATE RADIX-8 BOOTH MULTIPLIERS FOR LOW-POWER AND HIGH-PERFORMANCE OPERATION
- A HIGHLY SECURE FPGA-BASED DUAL-HIDING ASYNCHRONOUS-LOGIC AES ACCELERATOR AGAINST SIDE-CHANNEL ATTACKS
- DESIGN AND IMPLEMENTATION OF WALLACE TREE MULTIPLIER AND KOGGE STONE ADDER
- DESIGN FLOW FOR THE IMPLEMENTATION OF OBFUSCATED FINITE STATE MACHINES
- QUANTUM MODULAR MULTIPLICATION
- DESIGN AND IMPLEMENTATION OF AN IMPROVED CARRY INCREMENT ADDER
- AN OPTIMIZED M-TERM KARATSUBA-LIKE BINARY POLYNOMIAL MULTIPLIER FOR FINITE FIELD ARITHMETIC

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List of Projects

- DESIGN AND VERIFICATION OF 16 BIT RISC PROCESSOR USING VEDIC MATHEMATICS
- FULLY AUTOMATED TRAFFIC LIGHT CONTROLLER SYSTEM FOR A FOUR-WAY INTERSECTION USING VERILOG
- SCALABLE LOW-COST SORTING NETWORK WITH WEIGHTED BIT-STREAMS
- VLSI IMPLEMENTATION OF SPI AND I2C COMMUNICATION PROTOCOLS
- IMPLEMENTATION OF AES ALGORITHM ON FPGA AND ON SOFTWARE
- APPROXIMATE PARALLEL PREFIX ADDERS
- VLSI ARCHITECTURE OF S-BOX WITH HIGH AREA EFFICIENCY BASED ON COMPOSITE FIELD ARITHMETIC
- IMPLEMENTATION OF PIPELINED BOOTH ENCODED WALLACE TREE MULTIPLIER ARCHITECTURE
- A LOW-POWER AND HIGH-ACCURACY APPROXIMATE MULTIPLIER WITH RECONFIGURABLE TRUNCATION
- DESIGN AND ANALYSIS OF ENHANCED DADDA MULTIPLIER USING 5:2 COMPRESSORS

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List of Projects

- MODIFIED HIGH SPEED 32-BIT VEDIC MULTIPLIER DESIGN AND IMPLEMENTATION
- APPROACH FOR IMPLEMENTATION OF VENDING MACHINE THROUGH VERILOG HDL
- CONSTANT-TIME SYNCHRONOUS BINARY COUNTER WITH MINIMAL CLOCK PERIOD
- INEXACT SIGNED WALLACE TREE MULTIPLIER DESIGN USING REVERSIBLE LOGIC
- SAM: A SEGMENTATION BASED APPROXIMATE MULTIPLIER FOR ERROR TOLERANT APPLICATIONS
- DESIGN OF ULTRA-LOW POWER CONSUMPTION APPROXIMATE 4-2 COMPRESSORS BASED ON THE COMPENSATION CHARACTERISTIC
- DESIGN & IMPLEMENTATION OF WALLACE TREE MULTIPLIER AND KOGGE STONE ADDER
- LOW ERROR EFFICIENT APPROXIMATE ADDERS FOR FPGAS
- DESIGN OF ADVANCED ENCRYPTION STANDARD USING VERILOG HDL
- ANALYSIS OF LOW-DELAY IN 64-BIT VEDIC MULTIPLIER BASED MAC UNIT
- FPGA IMPLEMENTATION OF EFFICIENT AND LOW POWER TEST PATTERN GENERATOR
- DESIGN OF HIGH-ACCURACY SIGNED AND UNSIGNED RADIX 16 BOOTH MULTIPLIER

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- TRUNCATED BOOTH MULTIPLIER DESIGN OF APPROXIMATE COMPRESSORS USING VERILOG HDL
- IMPLEMENTATION OF FPGA SIGNED MULTIPLIER USING DIFFERENT ADDERS
- DESIGN FLOW FOR THE IMPLEMENTATION OF OBFUSCATED FINITE STATE MACHINES
- AREA-EFFICIENT LFSR-BASED STOCHASTIC NUMBER GENERATORS WITH MINIMUM CORRELATION
- DESIGN OF ULTRA-LOW POWER CONSUMPTION APPROXIMATE 4-2 COMPRESSORS BASED ON THE COMPENSATION CHARACTERISTIC
- A DESIGN AND IMPLEMENTATION OF HIGH SPEED IEEE-754 DOUBLE PRECISION FLOATING POINT UNIT BASED ON VEDIC TECHNIQUES
- DESIGN OF HIGH-SPEED APPROXIMATE ADDERS FOR FPGAS

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Eligibility

➢ B.Tech | M.tech | MS Students
➢ Above 70% Percentage
➢ Good Technical skills, Digital electronics, Verilog HDL, any Programming languages
➢ Problem Solving skills

Duration

➢ Internship work can be done in a period of 8-12 weeks.

Support

➢ Mentor will work with you to understand your goals and tailor their guidance to help you achieve them. Mentor will be there to provide solutions, tips, and strategies to overcome obstacles.

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Application

➢ Online application form will be available in the above registration link
➢ Online Application will be open from 10th May, 2024 to 20th May, 2024.
➢ Only 10 Candidates allowed for the Internship program

Program Fee

➢ The regular fee for the program is INR 15,000/- However, we are currently offering a discount!

Special Discount

➢ After discount applicable fee is **INR 4999/-**