SEMI DESIGN

RTL TO GDS DESIGN FLOW

Course Curriculum

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Visit Our Website
www.semidesign.in

RTL TO GDS DESIGN FLOW

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Week 1:

Session 1 : Full RTL to GDS Flow (Introduction to the entire flow)

- Key stages in the process (RTL design, synthesis, place & route, physical verification)

Session 2: Fabrication Flow

- Overview of the semiconductor fabrication process
- From GDSII to tapeout, including mask generation and silicon processing

Session 3: Linux Environment Setup & Basic Linux Commands

- Setting up the Linux environment for VLSI tools
- Cover basic Linux commands for file handling, navigation, and scripting

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Week 2:

Session 4-5: Basic TCL Commands

- Introduction to TCL scripting
- Essential TCL commands and usage in automation

Session 6: Tool Demonstration

- Introduction to all the open-source tools you'll use
- Overview of installation and configuration for the tools

Week 3:

Session 7-8: Bambu -> High-Level Synthesis

- Introduction to High-Level Synthesis (HLS)
- Practical demonstration using Bambu for HLS

Session 9: Verilog Basics

- Basics of Verilog for RTL design
- Syntax, structure, and coding guidelines

Week 4:

Session 10-11: Quartus prime, Modelsimulator -> Writing and Validating Verilog Code

- Introduction to Modelsimulator for simulation
- Writing, compiling, and running testbenches

Session 12-14: Yosys -> Logic Synthesis & Technology Mapping

- Detailed session on logic synthesis using Yosys
- Technology mapping and optimization techniques

Week 5:

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- Detailed session on logic synthesis using Yosys
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Session 15-18: OpenRoad -> Floorplanning, Placement, CTS, Routing

- Introduction to OpenRoad for floorplanning and placement
- Routing and clock tree synthesis (CTS)

Week 6:

Session 17-18: Magic -> Layout, Physical Verification

- Introduction to Magic for layout generation
- Running DRC and LVS for physical verification

Session 19-20: OpenSTA -> Static Timing Analysis

- Fundamentals of static timing analysis (STA)
- Using OpenSTA for timing verification

Week 7:

Session 21-22: KLayout -> Layout Viewing, Editing, and Verifying GDSII Files

- Introduction to KLayout for GDSII file manipulation
- Hands-on editing and verification of layout files

Session 23-24: Project Assignment

- Assign a practical project that involves the full RTL to GDS flow
- Provide project guidelines and evaluation criteria

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Week 8:

Session 25-26: RTL Design of UART Protocol

- Project Hands on experience with detailed explanation

Session 27: Project Assignment

- Assign a practical project that involves the full RTL Design & Verification
- Detailed explanation of a project

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