SEMI DESIGN

INTERFACING OF DMA CONTROLLER WITH RISC-V PROCESSOR AT SYSTEM ON CHIP(SOC) LEVEL

Course Curriculum

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Visit Our Website
www.semidesign.in

SOC LEVEL VERIFICATION - MODULE 1

DURATION - 14 DAYS (WEEKLY 6 HOURS)

- ASIC vs FPGA
- SOC Architecture and Methodology
- Different blocks involved in the SOC
- Functionality of Each block
- Teams involvement in the SOC Verification
- SOC over traditional IC
- SOC Verification Flow
- IP Verification
- Sub-system Verification
- SOC Verification
- Overview on SOC Level Verification involved with Processor verification

32-BIT RISC-V PROCESSOR DESIGN - MODULE 2

DURATION - 1 MONTH (WEEKLY 6 HOURS)

- History of RISC-V Processor
- Overview RISC-V Instruction Set Architecture
- RISC-V Pipeline Architecture
- Detailed Explanation of RV32I Instruction types
- Instruction set and Addressing modes
- Detailed Explanation of Registers and Instruction Formats
- R-Type, I-Type, S-Type, B-Type, J-Type, Instructions
- Instruction pipeline Hazards
- Detailed Explanation on Data Hazards, Control Hazards of RISC-V Pipeline
- Hands on Practice on Assembly Programs
- RISC-V Execution Stages and Pipeline
- In depth of Graphic processors
- Case study on GPU Architectures

32-BIT RISC-V PROCESSOR DESIGN - MODULE 3

DURATION - 1 MONTH (WEEKLY 6 HOURS)

- ALU Datapath for R-Type, I-Type, S-Type, B-Type, J-Type
- RTL Design of RISC-V Processor
- Verification of RISC-V Processor using SV | UVM
- Detailed explanation DMA Controller Architecture
- DMA Controller Architecture, Address mapping
- Hands on Design development by each team
- RTL Design of DMA Controller and UVM Verification
- Interfacing RISC-V 16 bit Processor with DMA Controller
- SV | UVM Verification of RISC-V with DMA Controller

SOC LEVEL VERIFICATION - MODULE 4

DURATION - 14 DAYS (WEEKLY 6 HOURS)

- Pre Silicon & Post Silicon Verification at SOC Level
- Different teams involvement
- Post Silicon debugging
- DFT vs DFD
- How to develop feature wise test plan, How to create the test cases
- Options in test.dv
- Switches required to avoid errors
- CPP options, Run commands
- What are the main steps to be followed which debugging error
- Importance of Regression
- How to run the Regression
- Test execution steps
- How to check TESTPASS/TESTFAIL, Error Signature, TESTID, TESTLOCATION

COURSE ASSISTANCE

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