SEMI DESIGN

PCIE PROTOCOL

Course Curriculum

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PCIE PROTOCOL - MODULE 1

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Session 1 : Background

PCI-X Introduction and architecture

Drawback of the PCI and PCI-X.

Pcie Protocol Overview

Serial and Parallel Protocol

Limitation of the PCI parallel Bus protocol.

Session 2 : PCIe Architecture Overview

How Pcie evolved

Difference b/w Pci and Pcie

PCIe Topology

PCIe Throughput

Device layer architecture (3-layer architecture).
packet flow through the layers overview only.
Major functionality of each layer(transaction, datalink,phy layer).

Session 3 : Configuration Overview
What is meant by BDF
PCI-Compatible Space
Extended Configuration Space.
Single-host and multi-host system (Differences).
Configuration Requests(type0 and type1)
Enumeration

Session 4 : Address Space & Transaction Routing.
Base address registers(BARs).
Configuration Space access : CAM,ECAM
Type0 header and Type1 header
BAR configuration in type1 and type0 Headers.
Base and Limit Registers in the Headers.
Registers Used For Address Routing.

Session 5 : TLP Routing Basics
ID Routing(ARI),Transaction Layer Feature
Explanation about packet-based protocol
Header Format/Type Field Encodings of TLP

Different types of TLP (Memory, Atomic ,IO, Config , Message)
Completion TLP Type, Completion Timeout
TlP Prefix Rules , TlP ordering Rules, ECRC error handling
Header format of the TLP (3DW and 4 DW differences).
Memory request TLP format and full flow through the layers

Session 6 : Flow Control in transaction layer
Flow Control Buffers and Credits .
Flow control Example , update FC frequency
Flow Control Initialization (DLCMSM state machine).
flow control mechanism working
Quality of Service (VC arbitration , Port arbitration)

Explain about Traffic class and virtual channels.
What is meant by TC-VC mapping and why we need that.
Port arbitration(switch and multifunction devices)

Session 7 : Transaction Ordering
Ordering Rules and Traffic Classes (TCs) .

Data link layer
DLLP Types, DLL Data integrity
Generic Data Link Layer Packet Format.
Different types of DLLPs and functionality.
Difference between TLP and DLLP.
ACK/NACK Protocol working using DLLPs

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Session 8A : Physical Layer - Logical (Gen1 and Gen2).

Physical Layer Overview

Transmit Logic Overview

Receive Logic Overview

Packet Format Rules

mux, Byte Striping, Scrambler Algorithm, 8b/10b Encoding, Differential Driver

Session 8B : Physical Layer - Logical (Gen1 and Gen2).

Receiver Logic's Front End Per Lane.

Lane-to-Lane Skew

8b/10b Decoder(disparity calculation).

Byte Un-Striping

Descrambler, physical layer error handling

Session 9 : Physical Layer - Logical (Gen3)
Encoding for 8.0 GT/s
what is meant by Ordered Set Blocks(all types overview)
transmitter Framing Tokens.
Scrambling and scrambling rules

Session 10 : Gen3 Physical Layer Receive Logic
Differential Receiver
Gen3 Physical Layer Receiver Details
Gen3 CDR Logic

Gen3 Elastic Buffer Logic
Physical Layer - Electrical

Physical Layer Electrical Overview
Differential Transmitter/Receiver
Voltage Margining

Session 11 : Physical Layer - Electrical.
Transmission with De-emphasis
Benefit of De-emphasis at the Receiver
Three-Tap Tx Equalizer
The Eye Test

Session 12 : Link Initialization & Training
Ordered Sets in Link Training(TS1 and TS2).
Link Training and Status State Machine (LTSSM).
Overview of each state in the LTSSM.
Detect State explanation
Polling State(each substate also explained).

Session 13 : Link Training and Status State Machine (LTSSM).
Configuration State
Link and lane Number Negotiation.
Detailed Configuration Substates.
Recovery State
Detailed Recovery Substates.

Session 14 : Recovery state

Recovery.idle.

Other LTSSM states

L0 and L0s state

L1 and L2

Hot reset and loopback

Disable state

Condition for the FSM to go for each state.

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Session 15 : Error Detection and Handling

PCIe Error Reporting
Error Classes(Correctable Errors and uncorrectable).
fatal and non-fatal errors
PCIe Error Checking Mechanisms
Error Checks by Layer
Error-Related Configuration Registers
How Errors are Reported
PCI-Compatible Error Reporting Mechanisms
Advanced Error Reporting (AER)

Session 16 : Interrupt Support

Two Methods of Interrupt Delivery

The Legacy Model

Virtual INTx Signaling

INTx Message Format

Mapping and Collapsing INTx Messages

Register related to interrupt.

Session 17 : System Reset

Two Categories of System Reset

Fundamental Reset

Hot Reset (In-band Reset).

Function Level Reset (FLR)

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Session 18A : Power Management

Introduction to PM and need of PM
System PM States
Device-Class-Specific PM Specs
How the LTSSM state affects while change the device PM state .
Active State Power Management (ASPM).
Software Initiated Link Power Management
The PME Message

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Session 19 :

PIPE

Logic Protocol Analyzers

Pcie Gen4 Updates

Session 20 :

Pcie Soc and IP Level Verification

Session 21 :

UVM Verification and testcases Development

Doubt Discussion session