SEMI DESIGN

JOB ORIENTED VLSI DESIGN VERIFICATION PROGRAM

Course Curriculum

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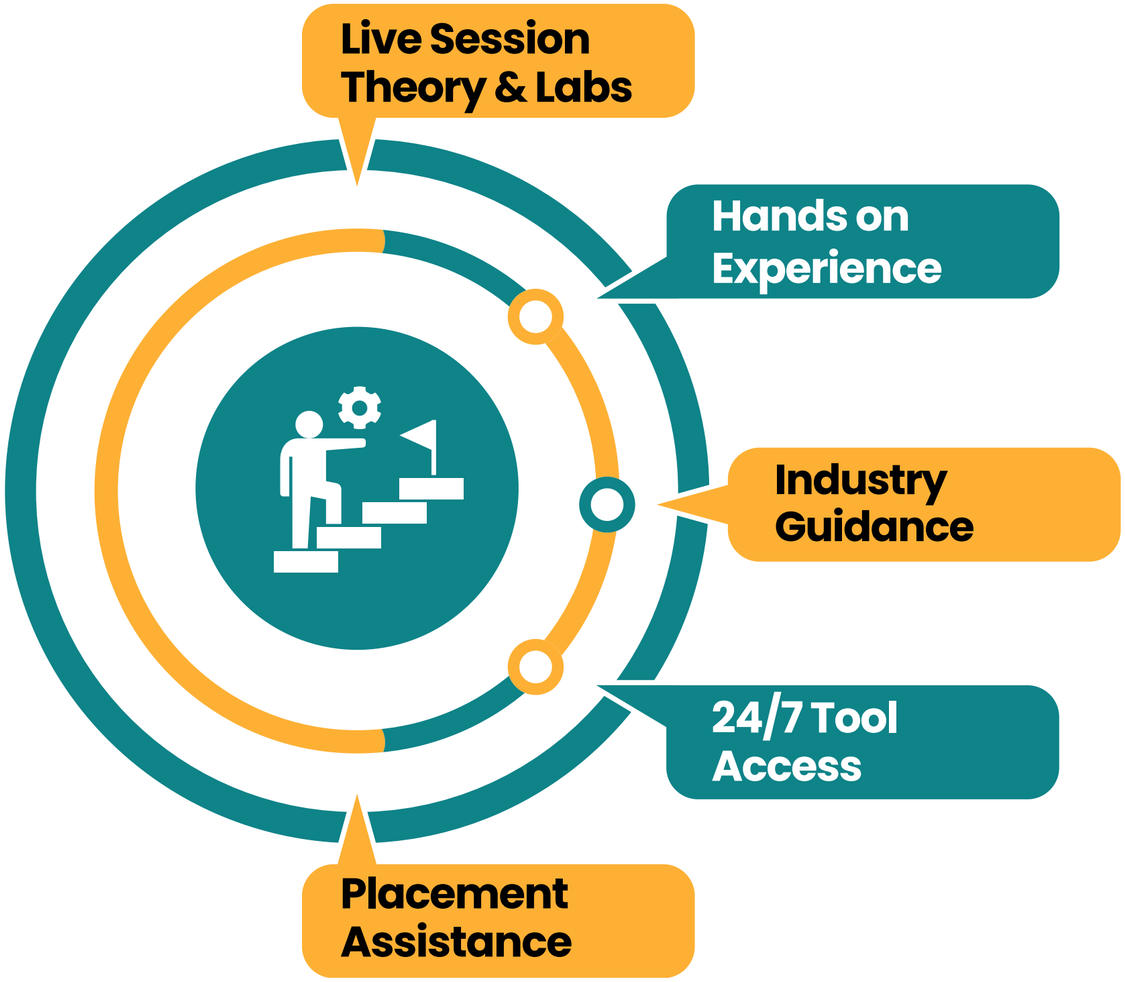
Visit Our Website
www.semidesign.in

DESIGN VERIFICATION COURSE - MODULE 1

DIGITAL ELECTRONICS

SEMI DESIGN

- Advanced level Digital Mocktests
- All type of Combinational Ckts
- All type of Sequential Ckts
- Registers
- Counters
- FSMs and Its Application examples
- Memories
- Static Timing Analysis
- CMOS Logic Design
- Glitches & Hazards
- Interview Preparation
- Assignments

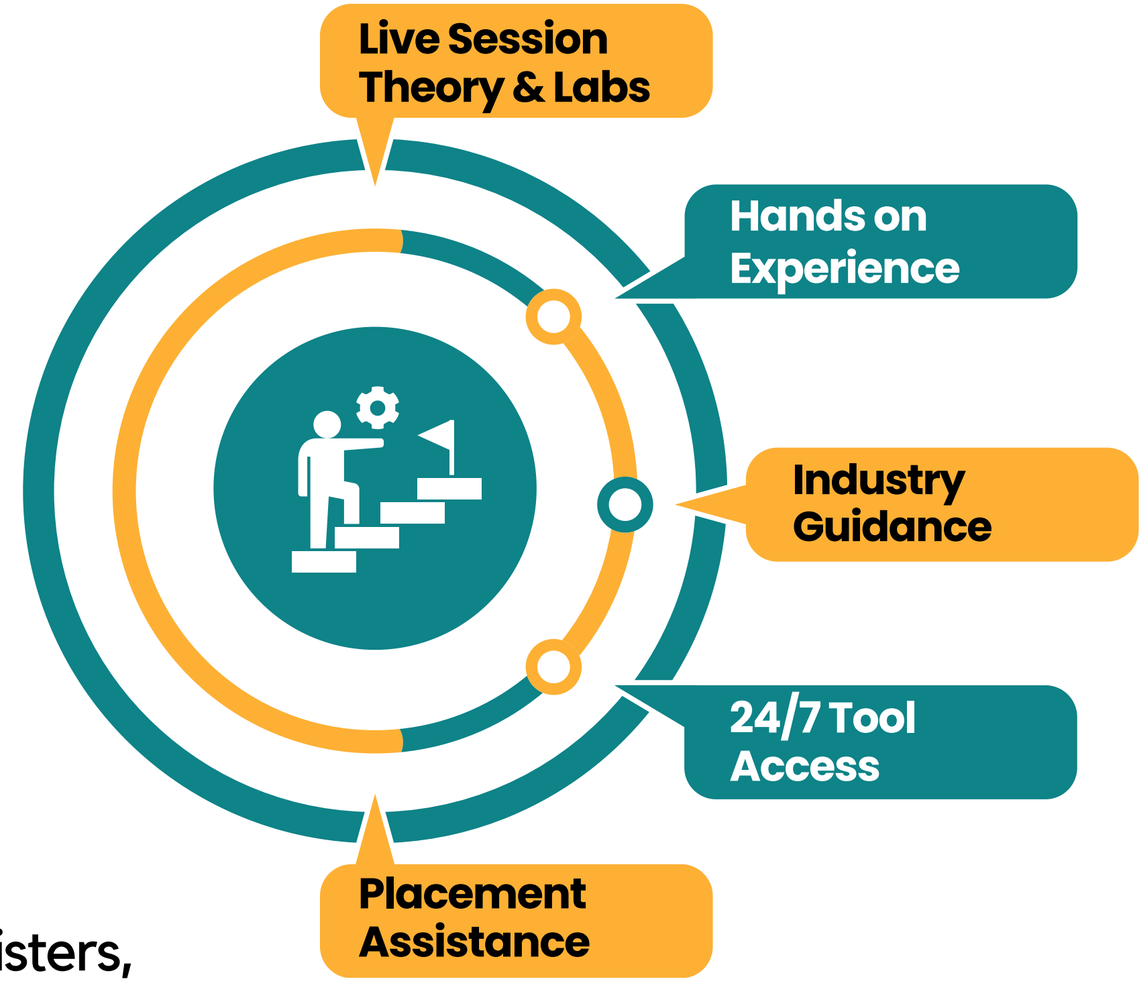


DESIGN VERIFICATION COURSE - MODULE 2

RTL DESIGN USING VERILOG HDL

SEMI DESIGN

- Language Introduction and Applications
- Data types, Operators
- All Description Styles
- Behavioral Modelling
- Dataflow Modelling
- Gate Level Modelling
- Switch Level Modelling
- Making Procedural Statements
- Making Continuus Statements
- Blocking and Non-Blocking Assignments
- Introducing the Process of Synthesis
- Coding RTL for Synthesis
- Modelling of Combinational, Flipflop, Registers, Counters

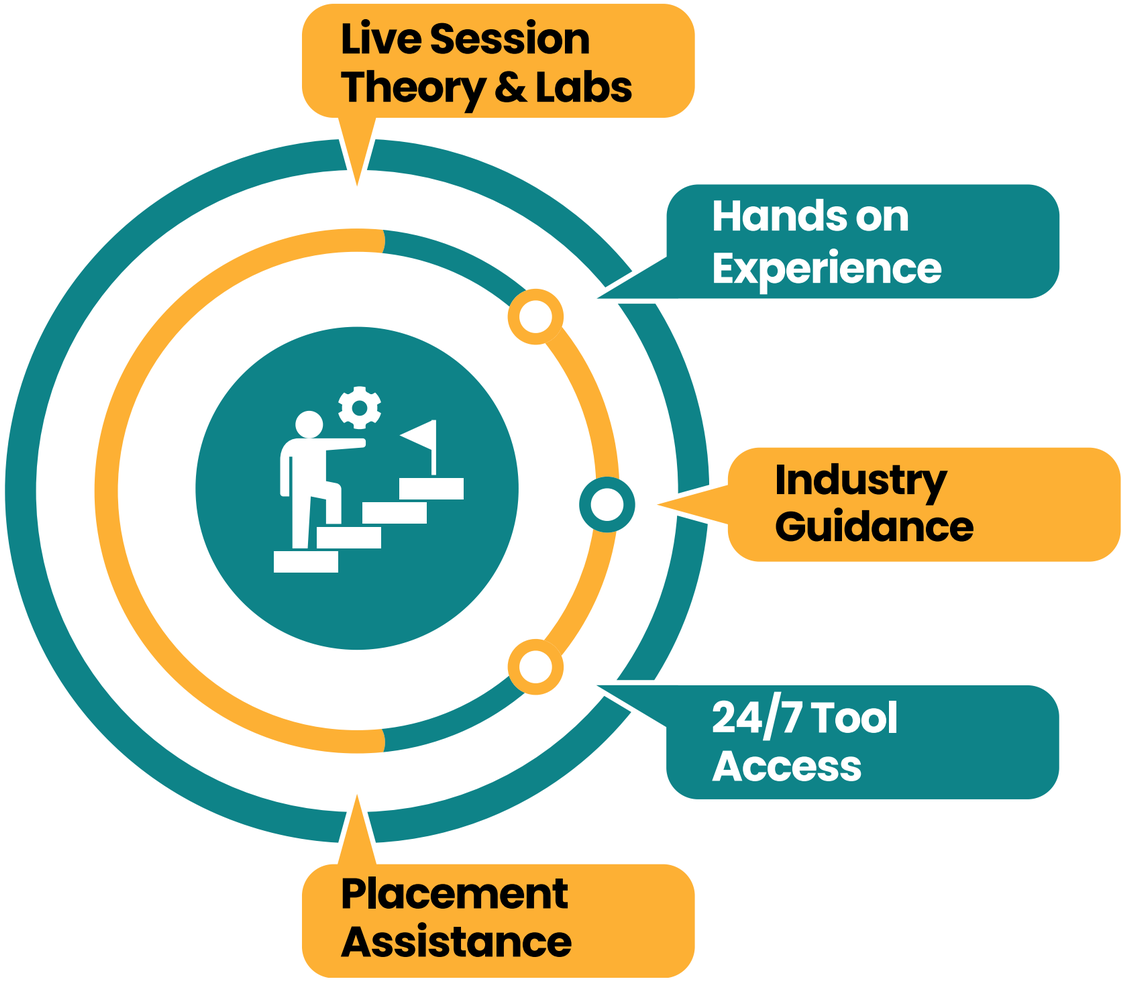


DESIGN VERIFICATION COURSE - MODULE 2

RTL DESIGN USING VERILOG HDL

SEMI DESIGN

- Designing Finite State Machines
- Understanding the Simulation Cycle
- Using Tasks & Functions
- Avoiding Simulation Mismatches
- Directing the Compiler
- Using Verification Constructs
- Coding Design Behavioral Algorithmically
- Coding and Synthesizing Examples
- Generating a Test Stimulus
- Developing a Testbench
- Using System Tasks and System Functions
- Example Verilog Testbench

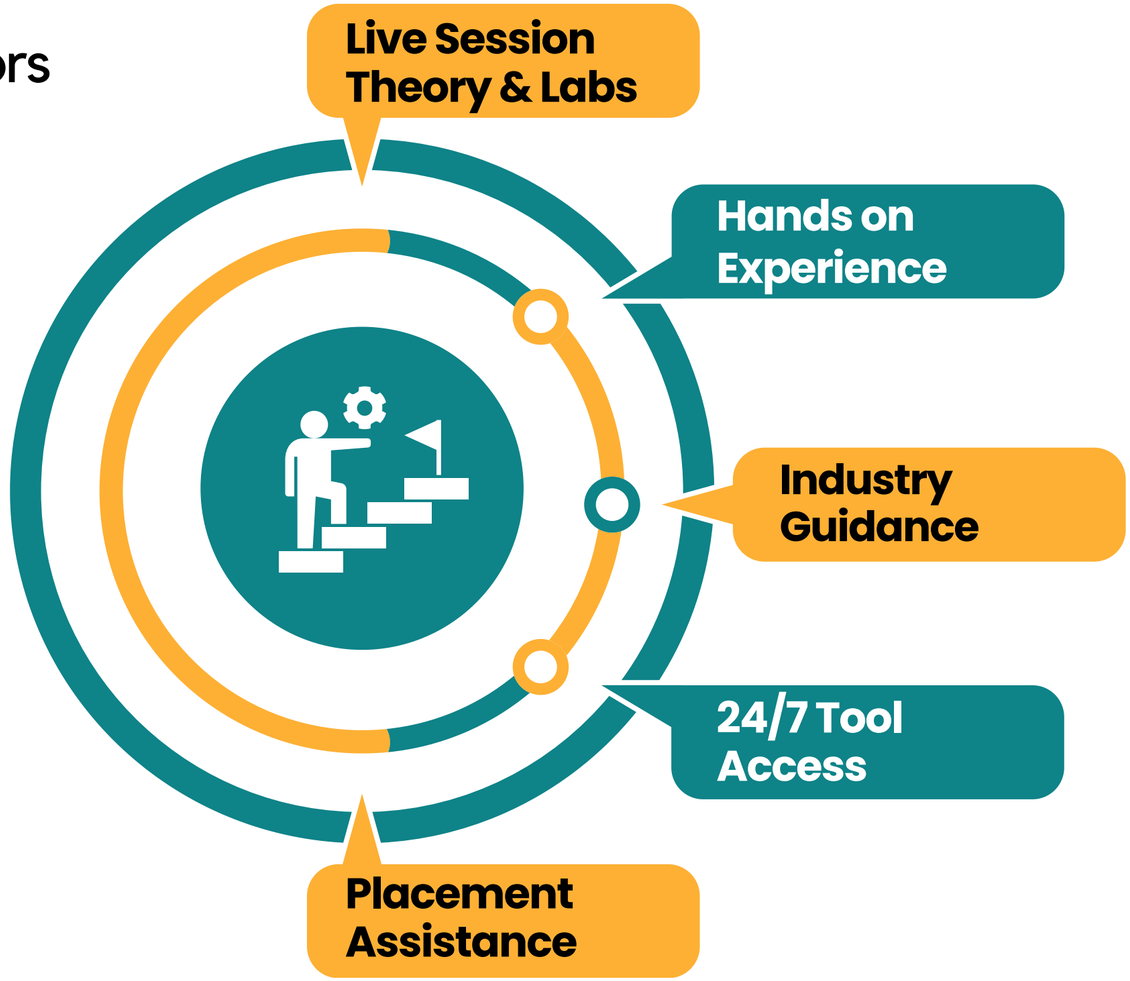


DESIGN VERIFICATION COURSE - MODULE 3

SYSTEMVERILOG (VERIFICATION)

SEMI DESIGN

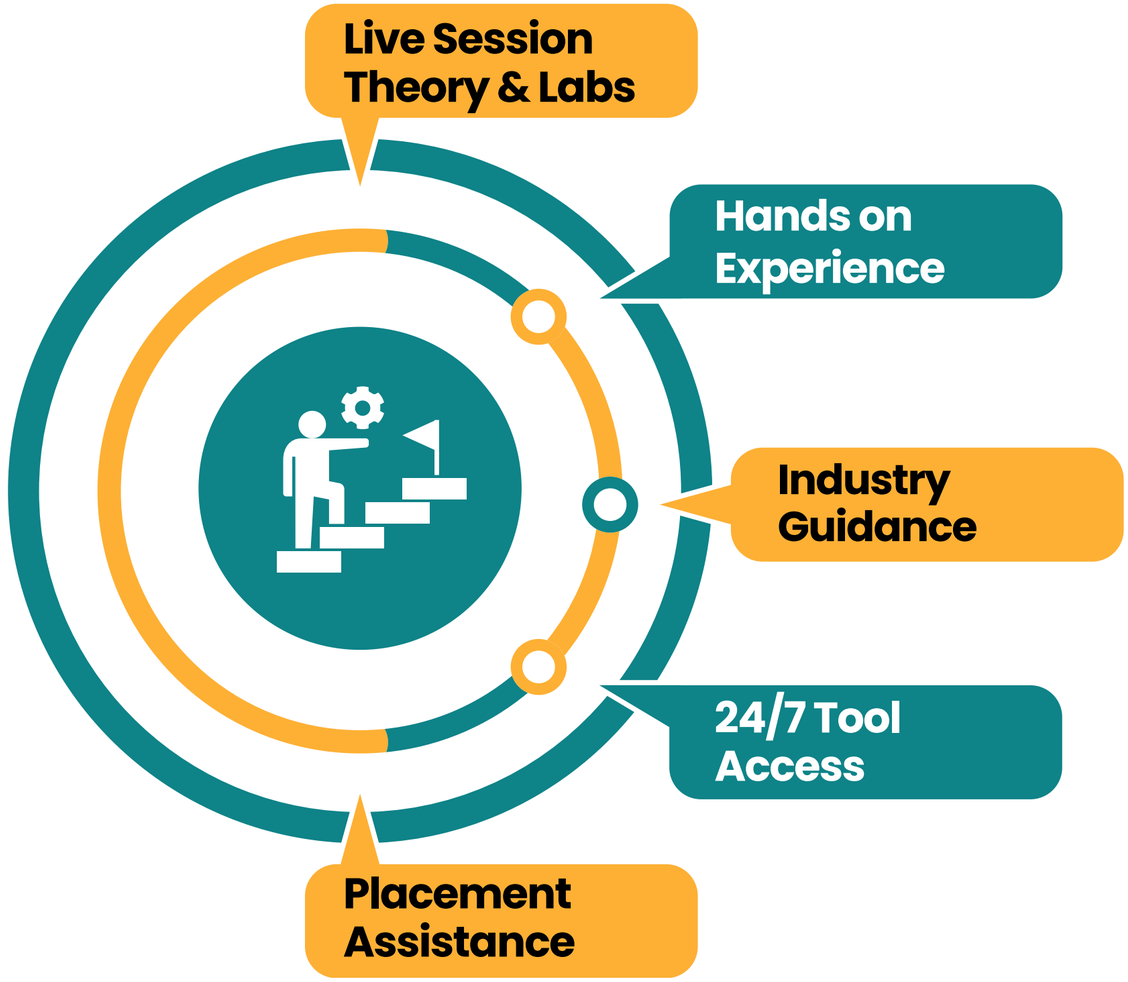
- SystemVerilog Overview
- Standard Data types & Literals & Operators
- User-Defined Data types & Structures
- Tb Architecture & Connectivity
- Testbench Components
- Static, Dynamic, Associative Arrays
- Queues
- Tasks & Functions
- Interfaces, Virtual Interface
- Verification Features
- OOPs, Classes
- Polymorphism and Virtuality
- Inheritance, Encapsulation
- Clocking Blocks



DESIGN VERIFICATION COURSE - MODULE 3

SYSTEMVERILOG (VERIFICATION)

- Clocking Blocks
- Random Stimulus
- Class-Based Random Stimulus
- Code Coverage
- Deep into Functional coverage
- Assertion Based Verification(ABV)
- SystemVerilog Assertions
- Direct Programming Interface(DPI)
- Interprocess Synchronization
- Testbench Components
- Testbench Examples
- Testplans, Testcases

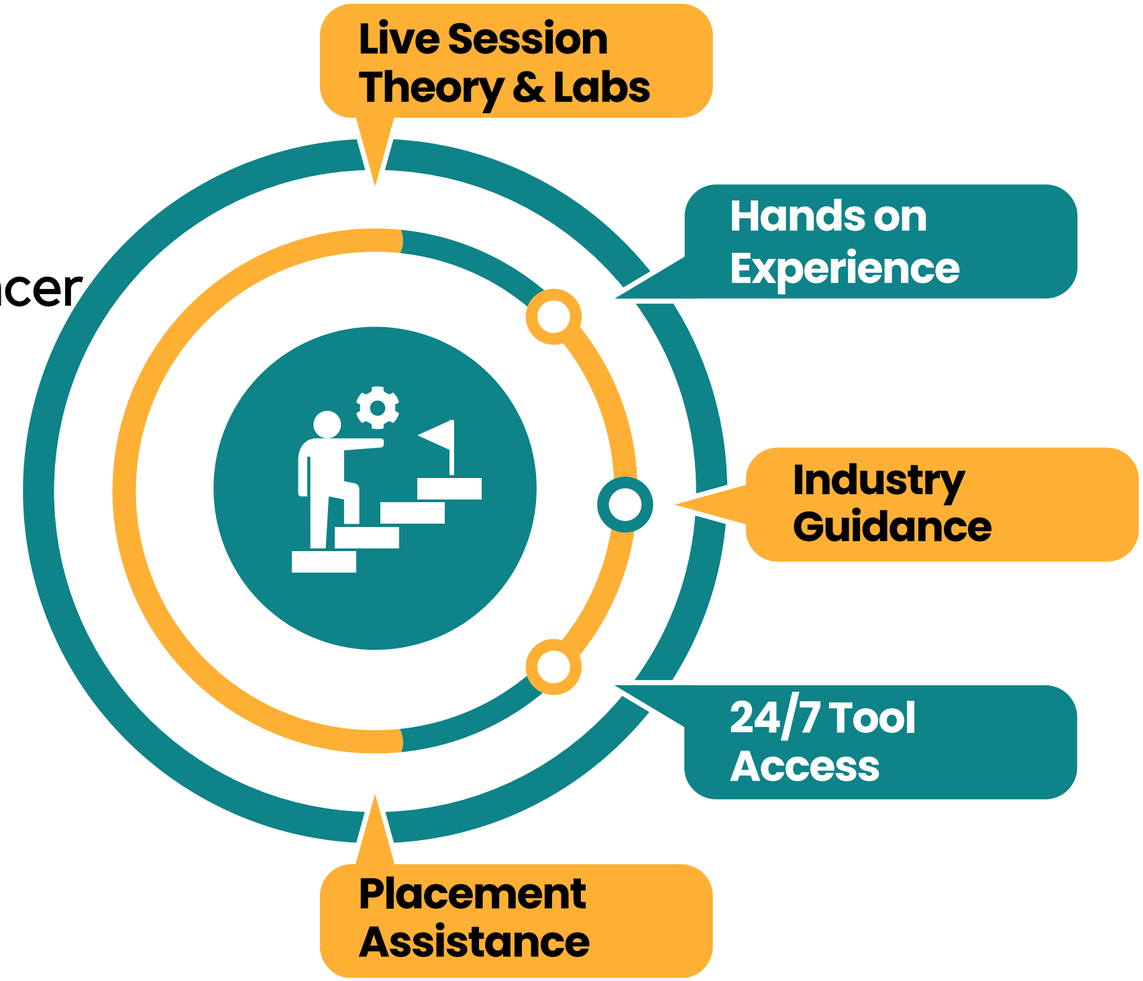


DESIGN VERIFICATION COURSE - MODULE 4

UVM (VERIFICATION)

SEMI DESIGN

- Deep understanding of UVM in SOC | IP
- Detailed explanation on UVC in SOC | IP
- Introduction to UVM, Features
- Testbench Hierarchy, Components
- UVM Sequence Item, Sequence, Sequencer
- Configuration, UVM config_db
- UVM Phases
- UVM Driver
- UVM Monitor
- UVM Agent
- UVM Scoreboard
- UVM Environment
- UVM Test
- Creating all components in a flow

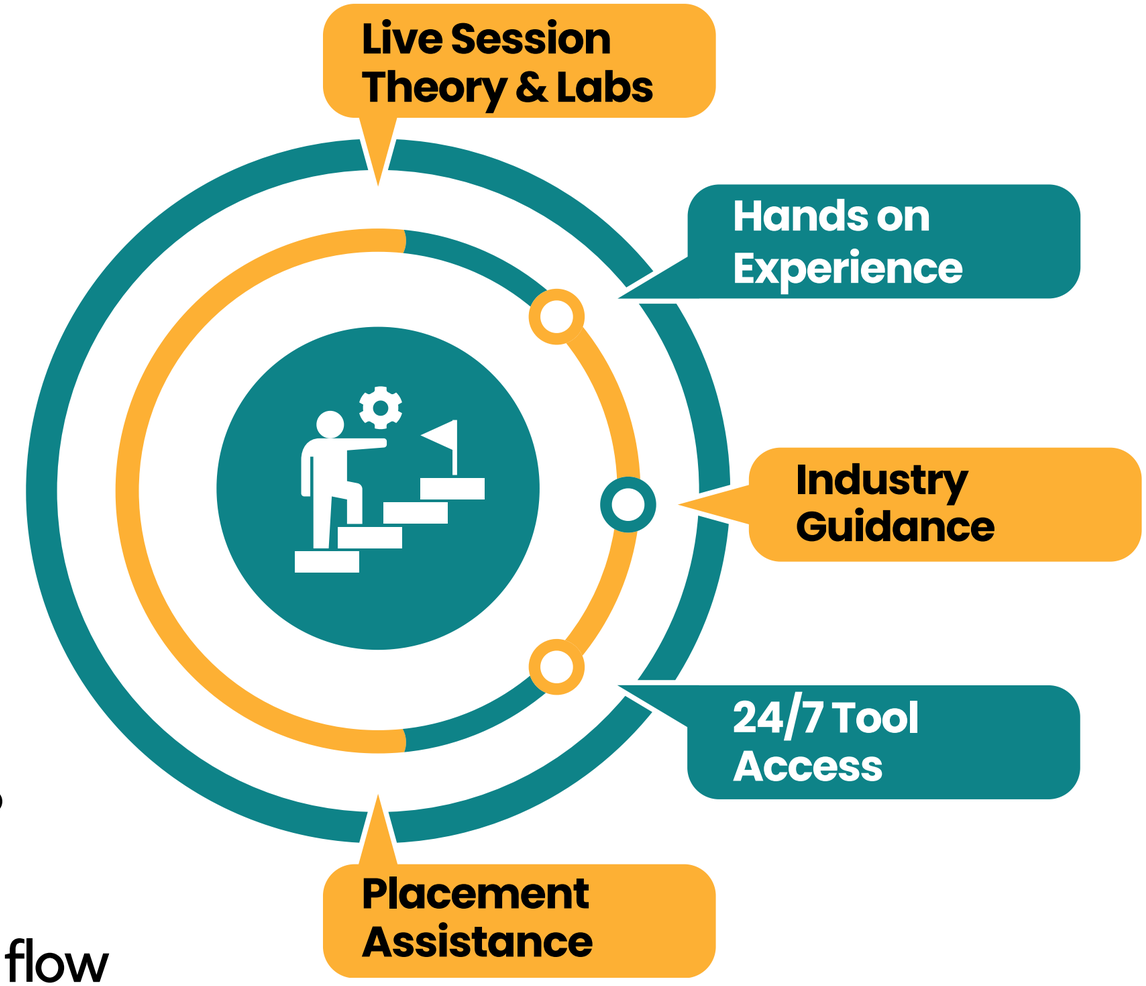


DESIGN VERIFICATION COURSE - MODULE 4

UVM (VERIFICATION)

SEMI DESIGN

- Understanding of UVM RAL Model
- Deep into UVM TLM
- Callback
- Events
- UVM Test
- UVM Testbench Examples
- UVM Testplan Creation
- DTPs(Detailed Test Plan Exaplanation)
- Testcase scenarios
- Importance of Regressions
- How to Run the Regression
- How to check test pass or fail in SOC | IP Level
- Idea on debugging testcases, execution flow



DESIGN VERIFICATION COURSE - MODULE 5

PROJECTS | PROTOCOLS

SEMI DESIGN

➢ RTL Design for UART Protocol, and detailed architecture implementation of Transmitter & Receiver
➢ RTL Design and Verification of 4-Port Calculator

➢ I2C Protocol Implementation & Verification using SystemVerilog

➢ AMBA (APB, AHB, AXI) Protocols RTL Design & Verification in SV & UVM
➢ Deep understand into Signal features of AMBA Protocols

➢ 1*3 Router Project in UVM Verification
➢ Detailed knowledge on Test plan development, writing test cases

➢ 4 Port Calculator RTL Design & UVM Verification

➢ DMA Controller Project with Coverage analysis, RTL design & Verification

DESIGN VERIFICATION COURSE - MODULE 6

PERL SCRIPTING

- Importance of Perl Scripting
- How to run the commands
- Idea on Coverage analysis
- Upload and extract the coverage report
- Walk through perl concepts
- Coding standards
- Explanation of Data types, Arrays
- Hashes, Loops
- Operators, Subroutines
- Date & Time
- References, Formats
- Directories
- Error Handling