SEMI DESIGN

DESIGN FOR TESTABILITY(DFT) PROGRAM

Course Curriculum

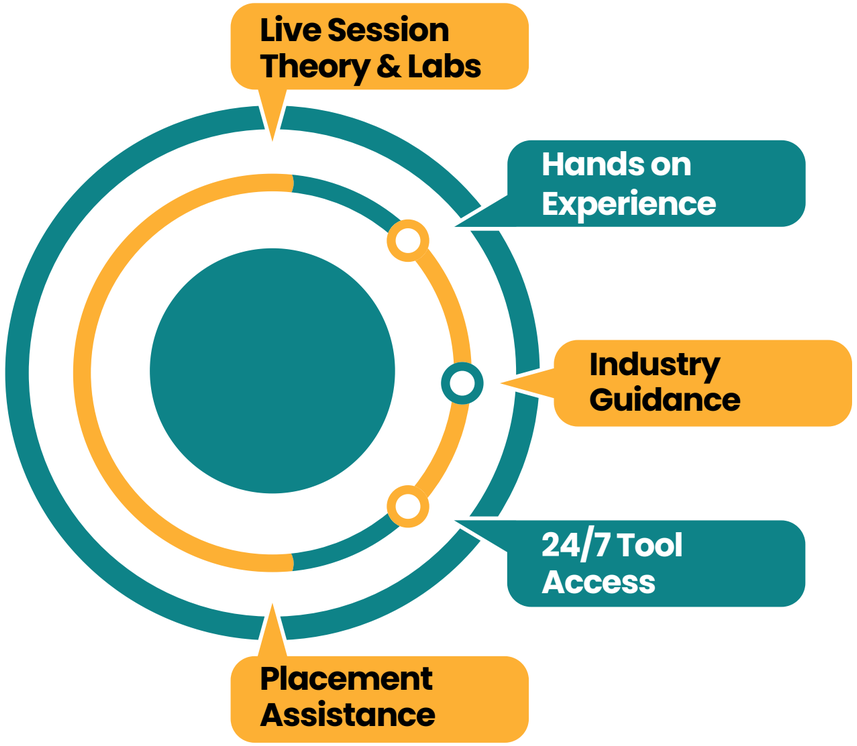
Phone Number
+91-9599745251

Visit Our Website
www.semidesign.com

DFT COURSE - MODULE 1

DIGITAL ELECTRONICS

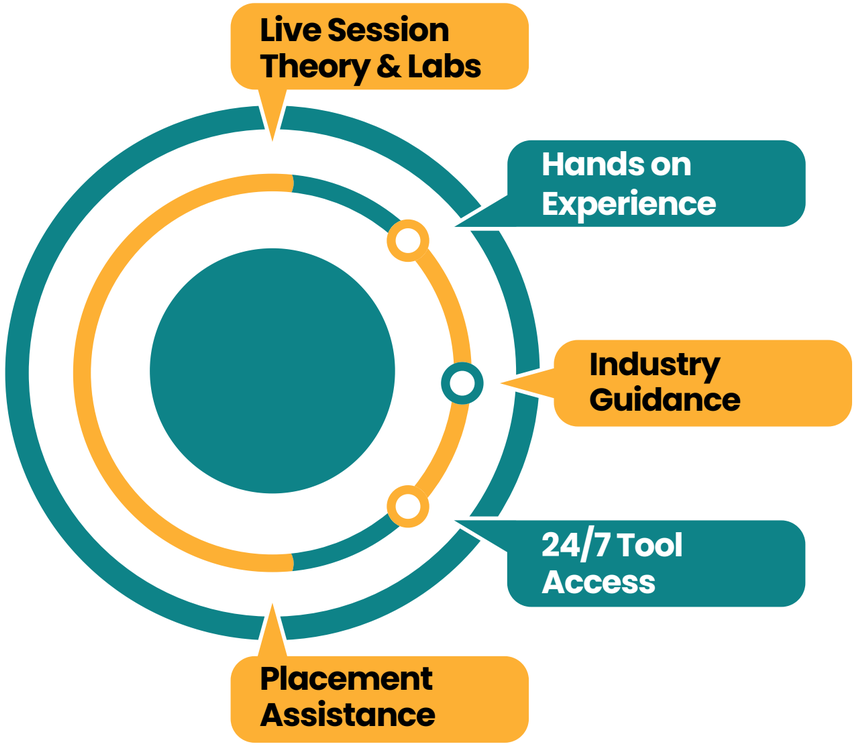
- Introduction to VLSI, ASIC Design flow
- VLSI Design Methodologies
- Advanced level Digital Mocktests
- All type of Combinational Ckts
- All type of Sequential Ckts
- Registers
- Counters
- FSMs and Its Application examples
- Memories
- Static Timing Analysis
- CMOS Logic Design
- Glitches & Hazards
- Interview Preparation, Assignments



DFT COURSE - MODULE 2

RTL DESIGN USING VERILOG HDL

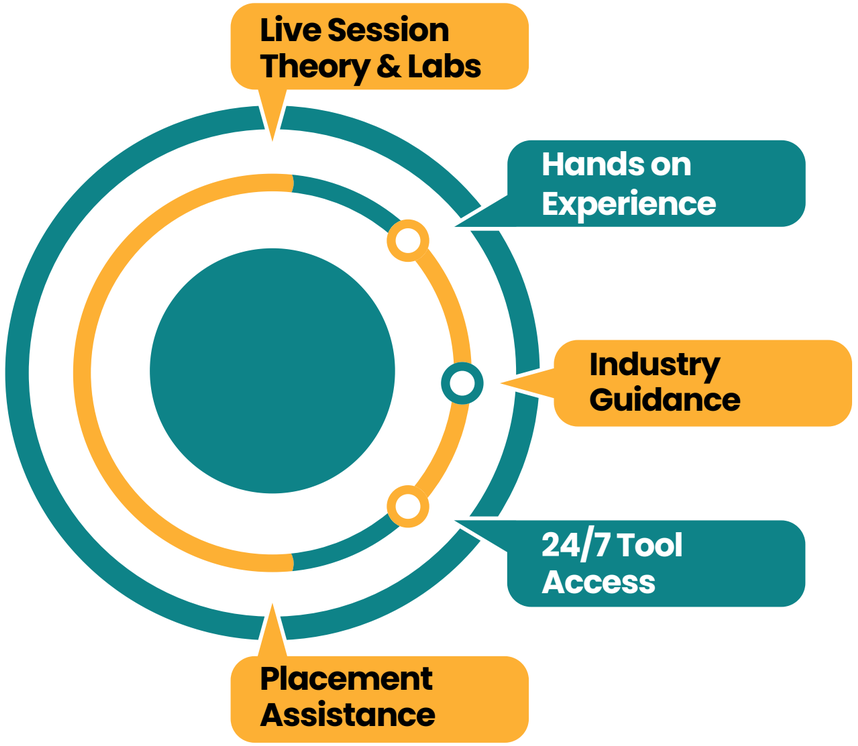
- Language Introduction and Applications
- Data types, Operators
- All Description Styles
- Behavioral Modelling
- Dataflow Modelling
- Gate Level Modelling
- Switch Level Modelling
- Making Procedural Statements
- Making Continuus Statements
- Blocking and Non-Blocking Assignments
- Introducing the Process of Synthesis
- Coding RTL for Synthesis
- Modelling of Combinational, Flipflop, Registers, Counters



DFT COURSE - MODULE 2

RTL DESIGN USING VERILOG HDL

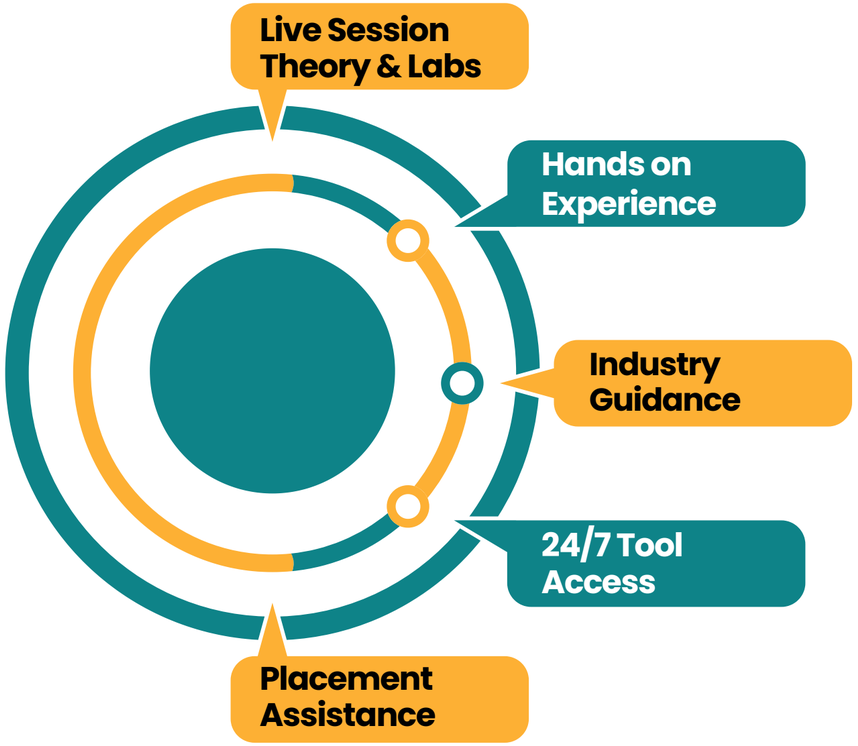
- Designing Finite State Machines
- Understanding the Simulation Cycle
- Using Tasks & Functions
- Avoiding Simulation Mismatches
- Directing the Compiler
- Using Verification Constructs
- Coding Design Behavioral Algorithmically
- Coding and Synthesizing Examples
- Generating a Test Stimulus
- Developing a Testbench
- Using System Tasks and System Functions
- Example Verilog Testbench



DFT COURSE - MODULE 3

CMOS DESIGN FUNDAMENTALS

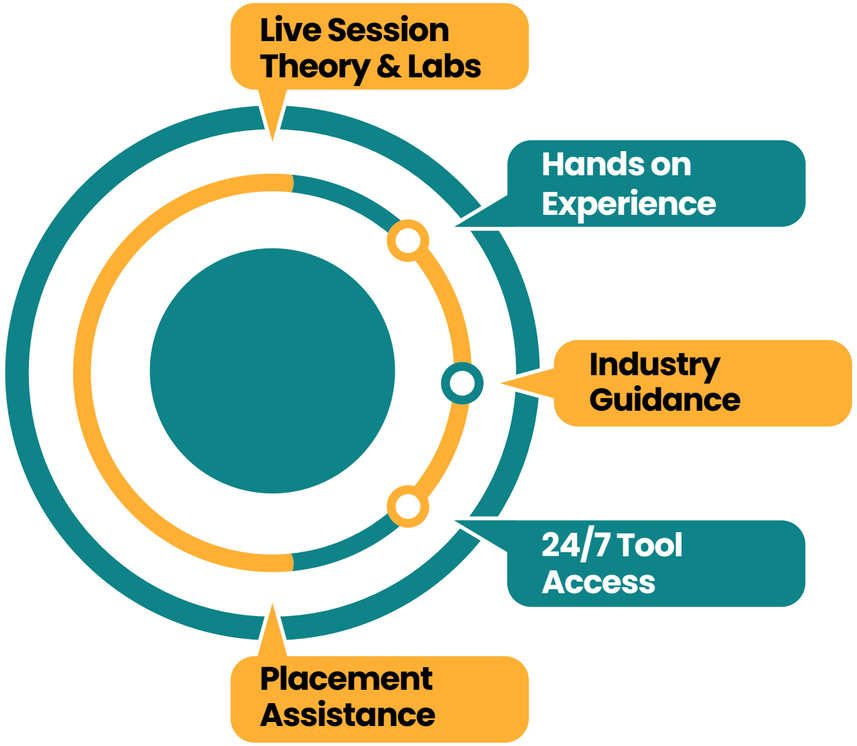
- Basic MOS Transistor
- Logic Gate CMOS Implementation
- Stick Diagram and Layout
- Process technology
- Power Dissipation for CMOS
- Parasitic Capacitance
- Second order Effect
- Scaling of MOS Circuits
- Layout and stick diagrams
- CMOS - Future trends



DFT COURSE - MODULE 4

DESIGN FOR TESTABILITY (DFT)

- DFT Design Flow
- Introduction to DFT,Features
- Roles of Testing
- Differentiating Design verification and DFT
- Design For Manufacturability
- Parameter YieldEstimation and Maximization
- Types of faults and models
- Testing Level
- Testing at different levels
- Fault modelling
- ATPG Basics
- Combinational ATPG, Additional fault models

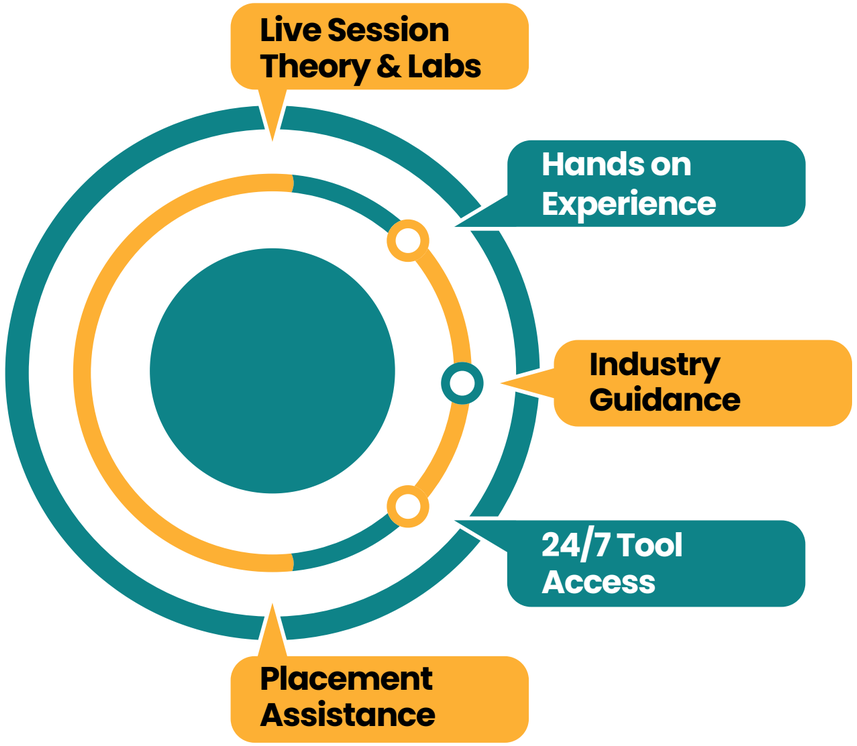


DFT COURSE - MODULE 4

DESIGN FOR TESTABILITY (DFT)

SEMI DESIGN

- Controllability and Observability
- BoundaryScan
- Introduction to ATPG and its Application
- Built-in Self Test (BIST) techniques
- Logis BIST
- Memory BIST
- Design Rule checks
- DFT Implementation on Practical examples
- Implementation of Memory controller Design
- Industry Scenarios approach



DFT COURSE - MODULE 5

PROTOCOLS & PROJECTS

- Introduction to the Protocols
- Protocols implementation in SOC | IP Level
- Different classification of Protocols
- UART, I2C, AMBA Protocols
- DFT Implementation of DMA Memory controller
- Industry based example
- Practical tool approach

- Introduction to Linux
- Commands and tool approach
- Perl Scripting