SEMI DESIGN

ADVANCED VERIFICATION PROGRAM

Course Curriculum

Phone Number
+91-9599745251

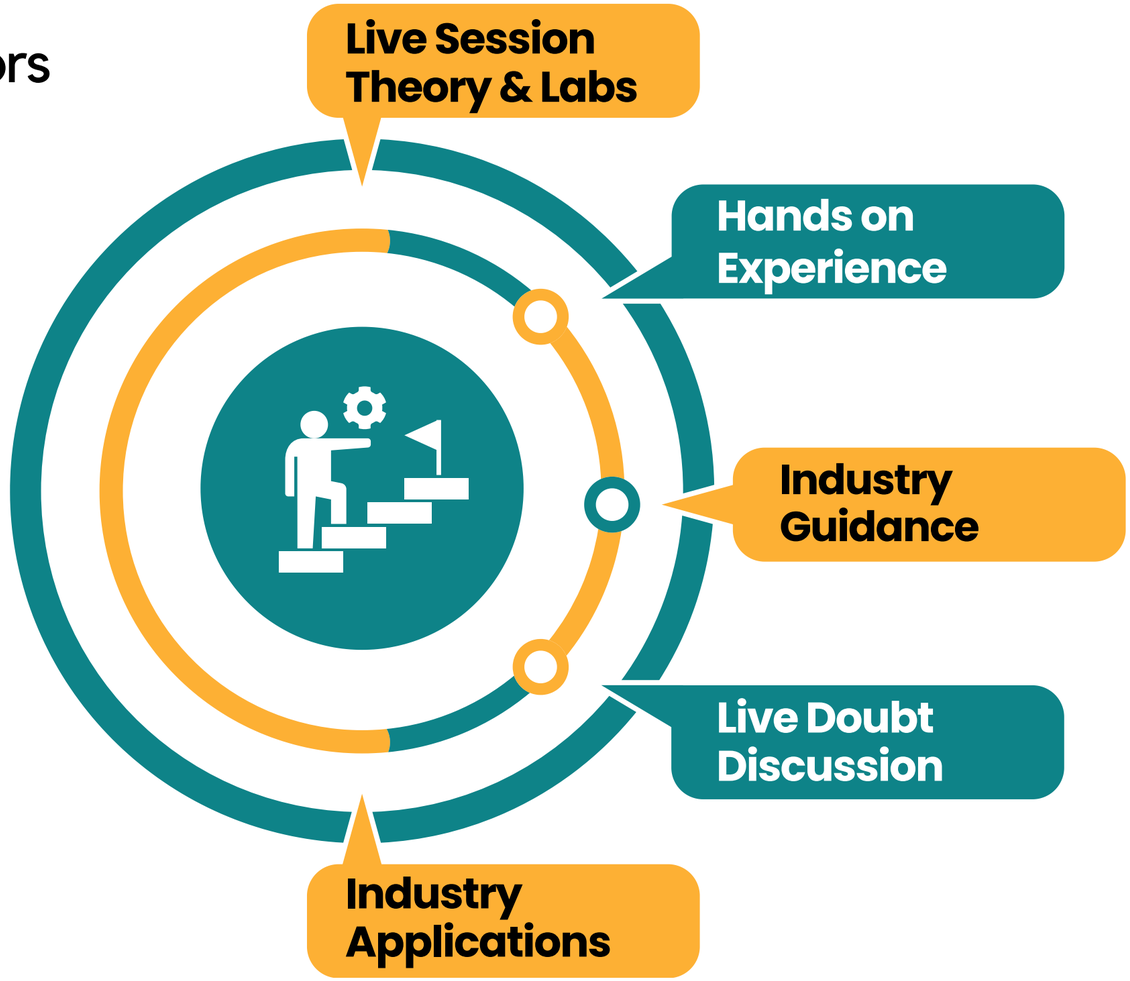
Visit Our Website
www.semidesign.com

ADVANCED VERIFICATION COURSE - MODULE 1

SYSTEMVERILOG (VERIFICATION)

SEMI DESIGN

- SystemVerilog Overview
- Standard Data types & Literals & Operators
- User-Defined Data types & Structures
- Tb Architecture & Connectivity
- Testbench Components
- Static, Dynamic, Associative Arrays
- Queues
- Tasks & Functions
- Interfaces, Virtual Interface
- Verification Features
- OOPs, Classes
- Polymorphism and Virtuality
- Inheritance, Encapsulation
- Clocking Blocks

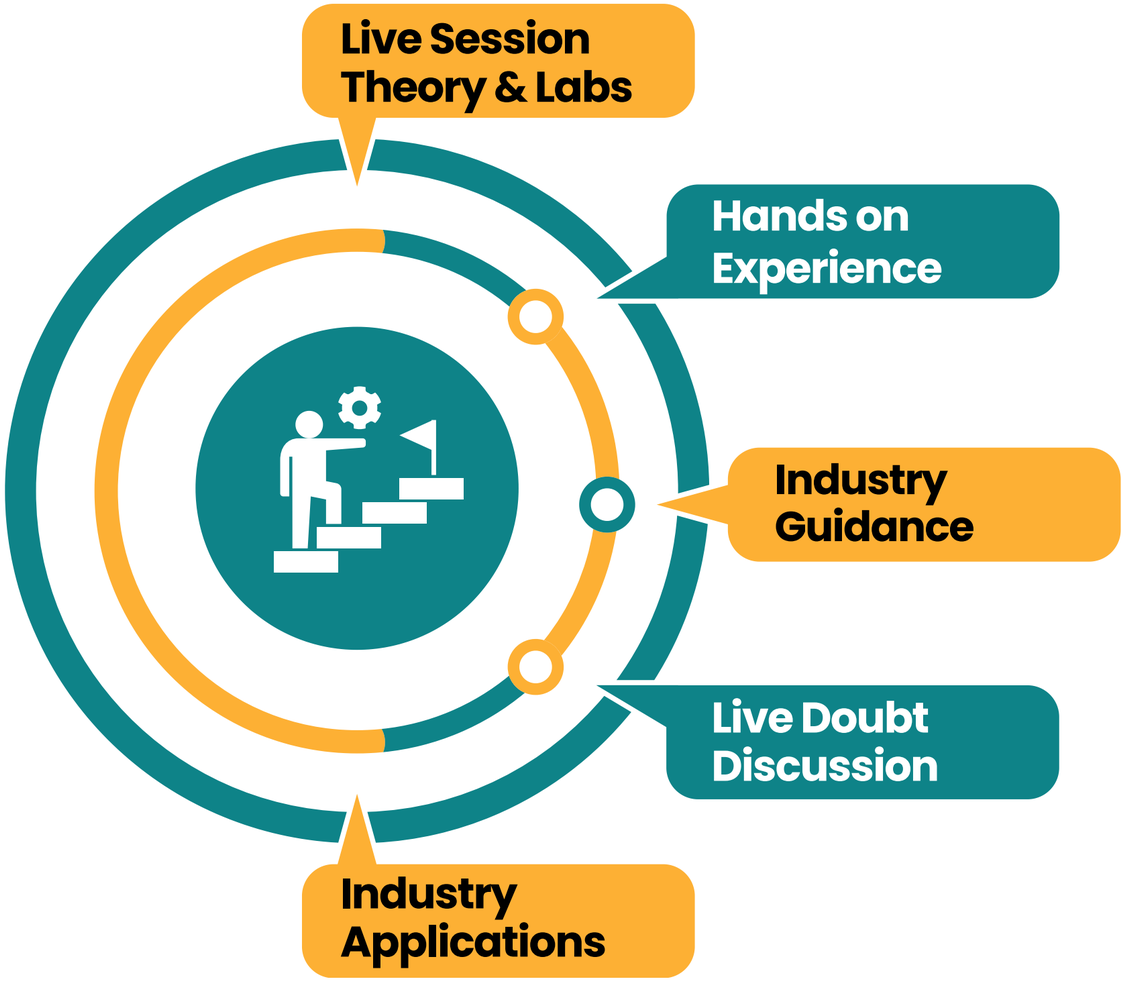


ADVANCED VERIFICATION COURSE - MODULE 1

SYSTEMVERILOG (VERIFICATION)

SEMI DESIGN

- Clocking Blocks
- Random Stimulus
- Class-Based Random Stimulus
- Code Coverage
- Deep into Functional coverage
- Assertion Based Verification(ABV)
- SystemVerilog Assertions
- Direct Programming Interface(DPI)
- Interprocess Synchronization
- Testbench Components
- Testbench Examples
- Testplans, Testcases

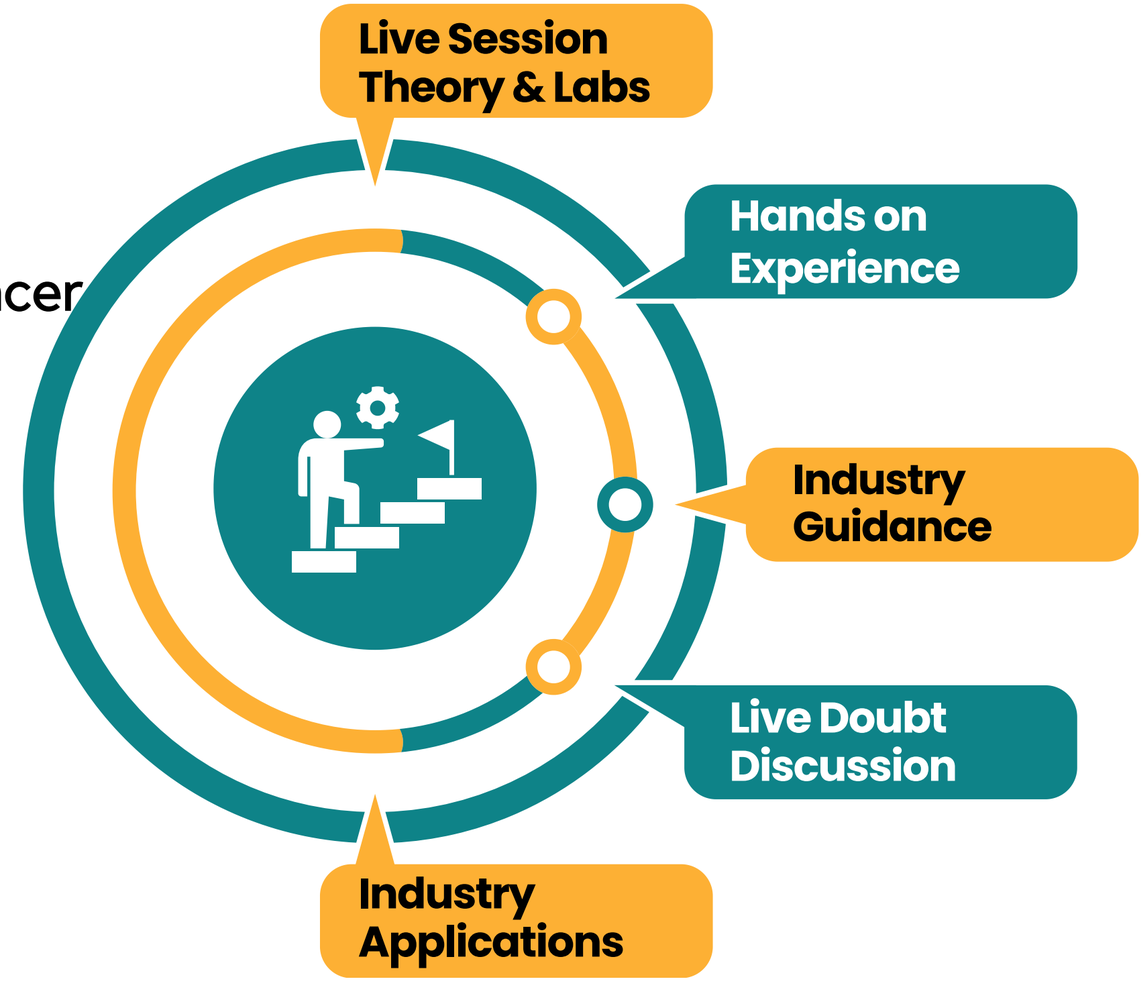


ADVANCED VERIFICATION COURSE - MODULE 2

UVM (VERIFICATION)

SEMI DESIGN

- Deep understanding of UVM in SOC | IP
- Detailed explanation on UVC in SOC | IP
- Introduction to UVM, Features
- Testbench Hierarchy, Components
- UVM Sequence Item, Sequence, Sequencer
- Configuration, UVM config_db
- UVM Phases
- UVM Driver
- UVM Monitor
- UVM Agent
- UVM Scoreboard
- UVM Environment
- UVM Test
- Creating all Components in a flow

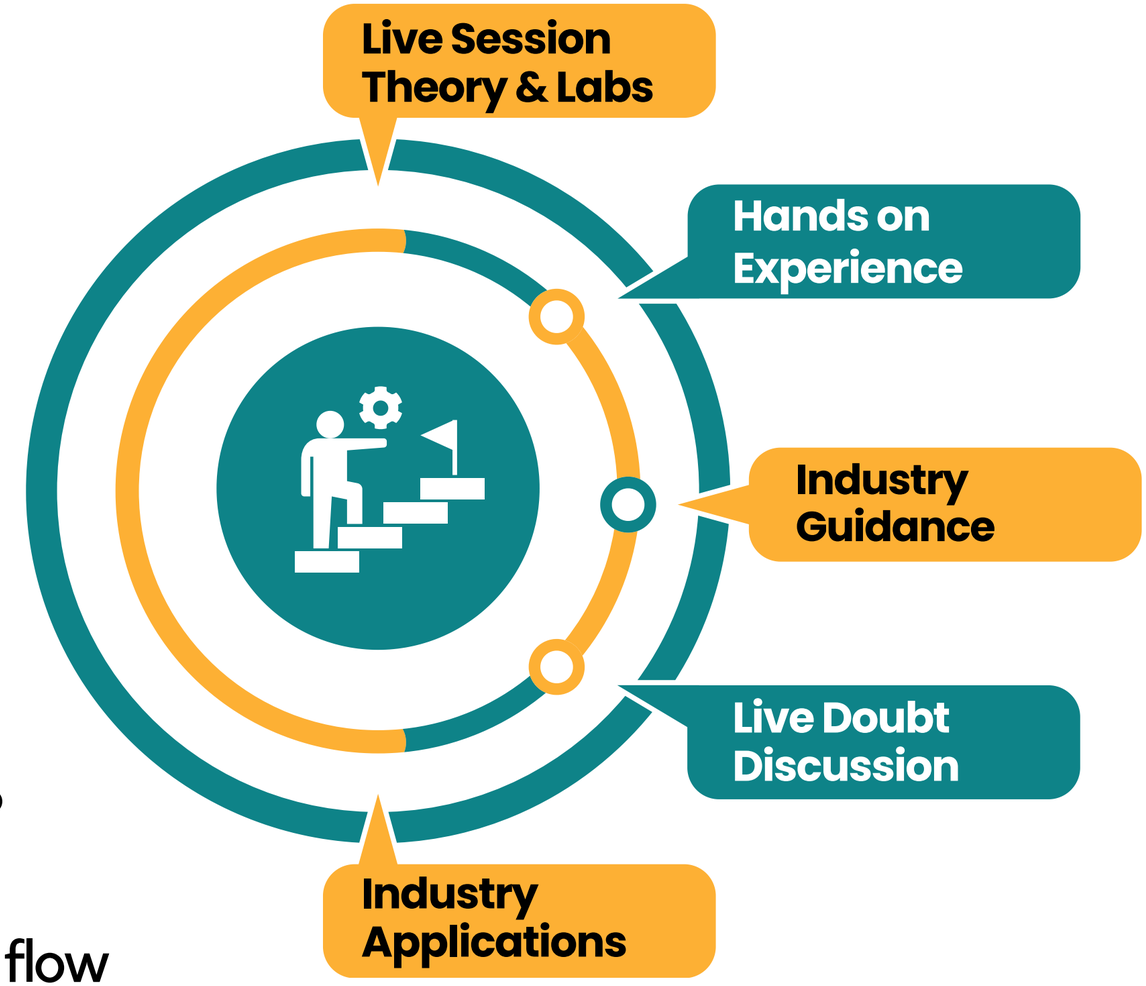


ADVANCED VERIFICATION COURSE - MODULE 2

UVM (VERIFICATION)

SEMI DESIGN

- Understanding of UVM RAL Model
- Deep into UVM TLM
- Callback
- Events
- UVM Test
- UVM Testbench Examples
- UVM Testplan Creation
- DTPs(Detailed Test Plan Exaplanation)
- Testcase scenarios
- Importance of Regressions
- How to Run the Regression
- How to check test pass or fail in SOC | IP Level
- Idea on debugging testcases, execution flow



ADVANCED VERIFICATION COURSE - MODULE 3

PROJECT | PROTOCOLS

➢ AMBA (APB, AHB, AXI) Protocols RTL Design & Verification in SV & UVM

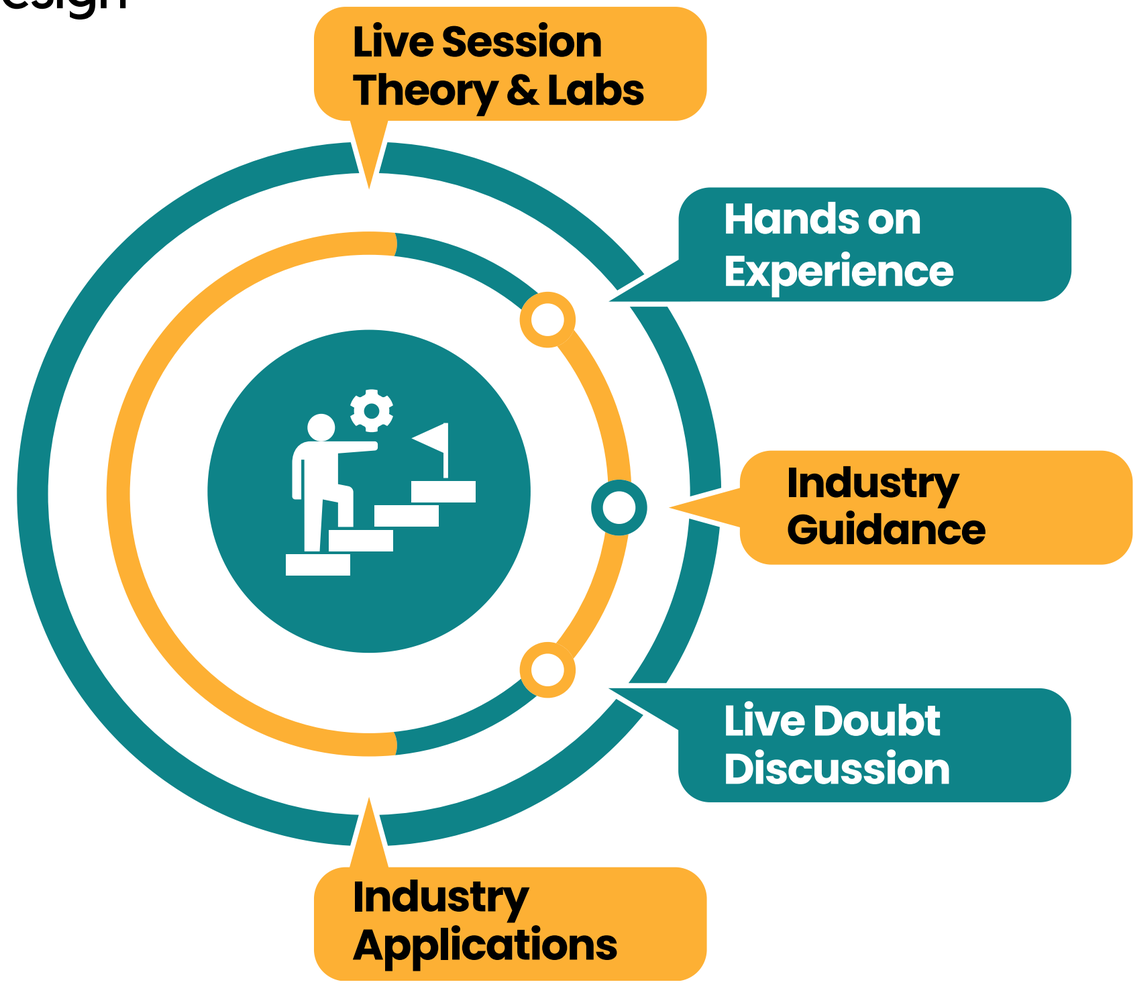
➢ Deep understand into Signal features of AMBA Protocols

➢ 1*3 Router Project in UVM Verification

➢ Detailed knowledge on Test plan development, writing test cases

➢ 4 Port Calculator RTL Design & UVM Verification

➢ DMA Controller Project with Coverage analysis, RTL design & Verification



ADVANCED VERIFICATION COURSE - MODULE 4

PERL SCRIPTING

- Importance of Perl Scripting
- How to run the commands
- Idea on Coverage analysis
- Upload and extract the coverage report
- Walk through perl concepts
- Coding standards
- Explanation of Data types, Arrays
- Hashes, Loops
- Operators, Subroutines
- Date & Time
- References, Formats
- Directories
- Error Handling