

RTL DESIGN & PHYSICAL DESIGN

15 Days Workshop Curriculum



Phone Number

+91-9599745251



Visit Our Website

www.semidesign.in

Day - 1

Introduction to VLSI, ASIC Design flow

Detailed discussion on Front-end domain & Back-end domain

RTL Design & Physical Design Overview

Day - 2

RTL Design using Verilog HDL

Synthesis & Simulation Hands on Lab sessions

Combinational Logic circuits discussion

Day - 3

Procedural assignment, Continuous assignment statements

Blocking & Non-blocking assignments

PROTOCOLS WORKSHOP



Day - 4

Sequential Logic circuits discussion

Registers, Counters - Part 1

Hands on Lab Sessions

Day - 5

Registers, Counters - Part 2

FSM Design using Verilog HDL, Lab session

Day - 6

FIFO memory RTL Design & Verification

Interview Questions Discussion

Day - 7

Introduction to PD flow and Importance of Linux in PD
CMOS Design examples

Day - 8

CMOS Design Advanced discussion
Construction of Basic gates using CMOS and analysis by Tanner
Interview Q/A Discussion

Day - 9

Synthesis flow part 1 and input files discussion
Synthesis flow part 2 (.lef/.lib/.upf/.spef)

Day - 10

Floorplan and .ndm library brief

Static Timing Analysis - part 1

Day - 11

STA part 2

Placement and Routing

Day - 12

Clock tree synthesis with Industry approach

Physical verification - Lab sessions

Day - 13

physical Signoff

tcl scripting, commands and script files

Day - 14

UART Protocol & Project Discussion

RTL Design & Lab Session

Day - 15

Interview Q/A Discussions

Assignment Q/A Discussion

Industry Approach

Required Projects

COURSE ASSISTANCE



Live Sessions

Batch starting from September 5th, 2024

Alternate days live sessions and assignment practice

Code Access

PPT and materials will be provided

Codes will be provided

Workshop fee

RTL Design & Physical Design in 1 Workshop - Fee 4999/-

Last date for registration September 1st, 2024