Semi Design Special Internship

DECEMBER 2021

Profile : RTL and Verification Intern 6 Months

Content & Prerequisites

Internship : 6 Months

Those who knows basics of Verilog, SV and UVM

1. Assignments will be given (Digital, Verilog, SystemVerilog and UVM)
2. Interview question preparation.
3. weekends, doubt classes will be taken.
4. An individual Mock interview will be conducted.
5. Have to develop UVM test bench from scratch for one project.
6. Assistance for one projects on protocols will be done.

Outcome :

1.will be prepared for interview.
2.will be able to Write UVM test bench.
3.will have idea about one protocol.

Those who knows basics of Verilog (Graduation/Post graduation final year student)

1. Assignments will be given (Verilog, Digital)
2. System Verilog basics & UVM basics Recorded lectures are available.
3. weekends doubt clear classes will be taken.
4. An individual Mock interview will be conducted.
5. Have to develop UVM test bench from scratch for one project.

Outcome :

1. Will be prepared for interview.
2. Will be able to Write UVM test bench.
3. Will have idea about Verification process.

Mentor and Advantages :

- This internship will run under guidance of working professional.
- Tool : EdaPlayGround or QuestaSim or Xilinx
- 6 Month Industry Real Time Experience Certificate
- Paid Work after Successful assessment & Industry Entry Help
- Share your application at info@semidesign.in

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