WORKSHOP CONTENT

HOW TO GET JOB IN VLSI
- DISCUSSION ON WHICH TOPICS SHOULD GET PREPARE FOR DESIGN & VERIFICATION INTERVIEW.

VERILOG :-
-DIFFERENT MODELLING STYLE.
- HOW TO WRITE SYNTHESIZABLE VARIABLE CODE.
-WHEN TO USE BLOCKING & WHEN TO USE NON-BLOCKING ASSIGNMENT.
- HOW TO AVOID SYNTHESIS & SIMULATION MISMATCHES FOR DESIGN.
- USE OF CASEX & CASEZ.

VERIFICATION METHODOLOGY
-HOW VERIFICATION IS DONE.
-IP, SOC VERIFICATION FLOW
-COVERAGE DRIVEN VERIFICATION
-FUNCTIONAL VERIFICATION
-CONSTRAINED RANDOM VERIFICATION
-DIRECTED & RANDOM TESTING

SYSTEM VERILOG
-FUNCTIONAL COVERAGE
-WRITING FUNCTIONAL COVERAGE FOR A PROJECT & CHECKING HOW TO INCREASE IT.
-WRITING ASSERTIONS
-CONSTRAINT EXAMPLES & DISCUSSION.

UVM
-UVM BASICS (SOME INTERVIEW RELATED QUESTIONS ON UVM BASICS WILL BE DISCUSSED)
-LEARN TO BUILD UVM TEST BENCH FROM SCRATCH (UVM DRIVER, UVM MONITOR, UVM SCOREBOARD ETC.)

PROTOCOL
-AXI PROTOCOL THEORY
-HOW TO CALCULATE ADDRESS IN AXI
-INTERVIEW QUESTIONS & ANSWERS DISCUSSION ON AXI

-QUIZ TEST AFTER EACH CONCEPT COMPLETION