Semi Design

find you way in #VLSI with us

Verilog HDL

Introduction to VLSI.

1. VLSI design flow (ASIC & FPGA)
2. VLSI methodologies.
3. ASIC ~ FPGA
4. Static timing analysis (basics)
5. Clock Domain Crossing.

Introduction to Verilog HDL

1. Basic concepts in Verilog.
2. Data Types.
3. Abstraction levels.

Dataflow modelling.

1. Continuous assignment.
2. Delays in Data Flow Modelling.
3. Structural Modelling
4. Writing test bench for the combinational circuit.

Behavioral modelling.

1. Procedural Blocks
2. Blocking & non-blocking assignments.
3. Verilog event scheduling.
4. Assignment execution order
5. Misconceptions about Nonblocking assignments
6. Blocking & Nonblocking assignment guidelines
7. Delays in behavioral modelling.
8. Race around conditions in Verilog.
9. Task & function.
10. Avoiding unwanted latches.
11. Synthesized result of code.

Memory modelling.

1. Single-port RAM modelling
2. Dual-port RAM modelling.
3. Synchronous FIFO design
4. Asynchronous FIFO design
5. Writing a self-checking test bench with different test scenarios to verification of the above designs.

FSM Design.

1. Moore & Mealy FSM.
2. Writing Verilog codes for FSM.
3. Different State machine coding style
4. One always block state machine coding style
5. Two always block state machine coding style
6. Three always block state machine coding style
7. Debugging FSM design.

Non-synthesizable constructs

1. Switch level Modelling.
2. UDP (User-defined primitives)
3. File handling in Verilog.
4. Writing test bench using File handling concept.
5. System task & compiler directive.
6. Continuous procedural assignment.
7. Specify block.
8. Timing checks in Verilog

Lab details

1. Basic LAB: writing design and self-checking Testbench for basic circuits such that adder, subtractor, Mux, Shift-Register, counter etc. (20 LAB questions)
2. Advance LAB: writing design and self-checking Testbench for the given specifications. (20 LAB question).

Project details

1. The project will explain with specification and coding.
2. Project specifications will be explained, assistance in coding provided**.**
3. **Project topic: UART, I2C, SPI, AMBA APB etc.**

Silent features

1. Individual Assistance granted for coding.
2. Daily interview oriented questions for Verilog as well as digital will discuss on Whatsapp.
3. After completion, of course, we are providing one-month extra assistance
4. Topic-wise knowledge test.

After completion of this course, you will:

1. Have a full understanding of the Verilog language
2. Understand the necessary constructs for synthesizable design.
3. Understand how to write a task-based self-checking test bench.
4. Know how to debug complex designs.
5. Know how to write and simulate data path and control path based designs.
6. Know the STA and CDC based concept.
7. Gain knowledge about protocols like AMBA (APB, AHB), UART, I2C, SPI etc.