Semi Design
find you way in #VLSI with us

UVM

UVM Module

- ❖ All about UVM
- ❖ What is UVM
- ❖ Why UVM
- ❖ Basic features of UVM
- ❖ Steps for downloading
- ❖ Books and websites to follow
- ❖ UVM TB - Building Blocks & their Relationship
  - Transaction Level Modeling
  - uvm_transaction
  - uvm_sequence_item
  - uvm_sequence
  - copying vs. cloning
  - macros and enum UVM_ALL_ON usage
- ❖ Customized TLM ports in UVM
  - TLM basics
  - Sequence-driver (PULL) interfaces uses seq_item_pull_port
  - PUSH model
  - PULL/PUSH model
  - Monitor-Subscriber – anaylysis_port
- ❖ Analysis Ports
  - adding more than one subscriber
  - usage of analysis_fifo
- ❖ OVM Factory
- ❖ Sequences
  - sequence life cycle
  - `uvm_do macros
  - virtual sequencer
  - parallel sequencer
  - sequencer arbitration
- ❖ Coordinated stimulus generation
  - virtual sequencer
- ❖ UVM Synchronization Mechanisms
  - uvm_event
  - uvm_barrier
  - uvm_objection
- ❖ Advanced Messaging
  - sending to multiple log files
  - promotion/demotion of severity

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- UVM configuration database
    - Config DB usage

Lab details

- Each topic is explained with proper code example.
- Basic LAB: Assignments based on each topic (Daily based, from each topic at least 5 questions.)
- Advance LAB: Assignment based on overall UVM. (more than one concepts are merged, that will help to understand how to apply the things you have learnt.20 Lab questions)

Project details

- 1 project will be explained with specification and coding.
- 1 project specifications will be explained, assistance in coding provided**.**
- Project topic: UART, I2C, SPI, AMBA APB etc.

Silent features

- Individual assistance provided for coding.
- Daily interview oriented questions for System Verilog will be discussed in what's app group.
- After completions of course 1 month assistance is provided in case you get any doubt
- Topic wise knowledge test. (Either Written or Telephonic)

After completion of this course, you will:

- Have a full understanding of the UVM language
- Have knowledge about writing efficient self-checking test bench using system Verilog language UVM.
- Have knowledge about object-oriented random stimulus generation & constraint random stimulus using class concept.
- Have knowledge about assertion based verification.
- Have knowledge about writing test bench with maximum functional coverage.

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