# Semi Design

find you way in #VLSI with us

## SystemVerilog HVL

### Introduction to Verification

- Why  System Verilog
- Verification Plan
- Different types of Verification Methods
- Directed testing Vs. Random testing.
- Basics of GLS (Gate level simulation)
- Assertion driven verification.
- Coverage driven verification

### Introduction to System Verilog

- Two state vs. four state data type.
- Data types
- Static & dynamic type-casting
- Task & Function
- Threads
- operators
- Enhanced loops & jumping statements
- Different types always block.
- Case & if statements
- time unit & time precision

### Oops Concept.

- Class basics .
- Different Copy methods.
- Inheritance
- Polymorphism
- Encapsulation.

### Randomization & constraint

- Randomizing variables.
- Randomizing object.
- Built in randomization methods.
- Randomization using constraint.
- Different types of constraints.
- External constraints
- Writing different test cases for different scenarios.

## Interface & Program block

- Interface overview.
- Interface constructs.
- Virtual Interface.
- Mod port
- Clocking block
- Program block
- Event scheduling in System Verilog

## IPC.

- Event control
- Semaphore
- Mail box.

## Building verification environment

- Verification environment for combinational circuits.(Adder, Encoder, Mux)
- Verification environment for sequential circuits.(Counter, RAM ,FIFO)
- BFM

## Coverage

- Code coverage
- Functional coverage
- Cover groups
- Cover points
- Cover point bins
- Cross coverage
- Adding coverage for above mentioned verification environment.

## Assertion

- Why assertion?
- Assertion types
- Immediate assertions
- Concurrent assertions
- Assert & cover properties
- Properties and assert property
- Implication operator.
- Assertion system functions
- Assertion severity tasks
- Writing assertion for above mentioned verification environment.

## Last Topics

- Direct Programming Interface
- Call Back
- Regression testing.

## Lab details

- Each topic is explained with proper code example.
- Basic LAB: Assignments based on each topic (Daily based, from each topic at least 5 questions.)
- Advance LAB: Assignment based on overall System Verilog. ( more than one concepts are merged, that will help to understand how to apply the things you have learnt.20 Lab questions)

## Project details

- 1 project will be explained with specification and coding.
- 1 project specifications will be explained, assistance in coding provided.
- Project topic: UART, I2C, SPI, AMBA APB etc.

## Silent features

- Individual assistance provided for coding.
- Daily interview oriented questions for System Verilog will be discussed in what's app group.
- After completions of course 1 month assistance is provided in case you get any doubt
- Topic wise knowledge test. (Either Written or Telephonic)

After completion of this course, you will:

- Have a full understanding of the System Verilog language
- Have knowledge about writing efficient self-checking test bench using system Verilog language.
- Have knowledge about object-oriented random stimulus generation & constraint random stimulus using class concept.
- Have knowledge about assertion based verification.
- Have knowledge about writing test bench with maximum functional coverage.