Semi Design

find you way in #VLSI with us

Static Time Analysis

- Introduction to STA
- STA in Design Flow
- Different Timing Paths
- Delays Review
- Combinational Delay
- Setup/Hold Requirement
- Clock to Q Delay
- Data Required Time
- Data Arrival Time
- Setup/Hold Violations
- Setup Check
- Hold Check
- Frequency Calculation
- Lab Sessions
- Exercises
- Mock test daily after session