Semi Design

find you way in #VLSI with us

CMOS DESIGN

1) Introduction to VLSI
    a. Moore's Law
    b. SoC
    c. VLSI Design Flow & Design Cycle
2) MOS Fabrication
    a. Lithography, Etching, Ion Implantation
    b. CMOS Fabrication, Well Creation
    c. Layout Design Rules
3) MOS Transistor Model & Analysis Under External Bias
    a. Energy Band Diagrams
    b. Accumulation, Depletion & Inversion
    c. Threshold Voltage
    d. I-V Characteristics
    e. Substrate Bias Effect
    f. MOS Scaling & Small Geometry Effects
    g. MOS Capacitances
4) MOS Inverters: Static Characteristics
5) MOS Inverters: Switching Characteristics
6) Calculation of Delay
7) Combinational MOS Logic Circuits
    a. NAND2 Analysis
    b. NOR2 Analysis
    c. CMOS Transmission Gate
8) Sequential MOS Logic Circuits
    a. SR Latch, JK Latch, D-Latch
    b. Setup, Hold and Clock to Q Delay
9) CMOS Family
    a. Pseudo NMOS, Pseudo PMOS
    b. Dynamic Logic
    c. CMOS Transmission Gate
10) Semiconductor Memories
    a. SRAM
    b. DRAM
11) Low Power CMOS Logic Circuits
    a. Dynamic, Static, Leakage & Short Circuit Power
    b. Techniques to design low power circuit